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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

2269-5565.1US

Application Number

10/826,985

Filed

April 19, 2004

VIA ELECTRONIC FILING

April 28, 2008

First Named Inventor

Shijian Luo

Art Unit

2823

Examiner

J. Stark

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record. 38,581
Registration number

☐ attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34


Signature

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Typed or printed name

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Telephone number

April 28, 2008

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below.

☐ *Total of forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Luo et al.

Serial No.: 10/826,985

Filed: April 19, 2004

For: METHODS FOR FORMING
PROTECTIVE LAYERS ON
SEMICONDUCTOR DEVICE
COMPONENTS SO AS TO REDUCE OR
ELIMINATE THE OCCURENCE OF
DELAMINATION THEREOF AND
CRACKING THEREIN

Confirmation No.: 3493

Examiner: J. Stark

Group Art Unit: 2823

Attorney Docket No.: 2269-5565.1US

VIA ELECTRONIC FILING
April 28, 2008

PRE-APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiners:

This Pre-Appeal Brief follows the final Office Action of January 28, 2008, and the Advisory Action of April 15, 2008. This Pre-Appeal Brief is being submitted with a petition for extension of time and the appropriate fee, and in accordance with the requirements of the Pre-Appeal Brief Conference Pilot Program (*see* 1296 Off. Gaz. Pat. Office 67, July 12, 2005) and is being submitted concurrently with a Notice of Appeal.

REMARKS

Claims 1-23 and 25-29 are currently pending and stand finally rejected in the above-referenced application.

The following grounds of rejection are presented in the final rejection:

(A) Independent claim 1 and its dependent claims 2-8, 19-23, and 25-29 have been rejected under 35 U.S.C. § 103(a) (claim 24 was previously canceled without prejudice or disclaimer) for reciting subject matter that is allegedly anticipated by the subject matter described in U.S. Patent Application Publication 2003/0171456 of Tong et al. (hereinafter "Tong"); and

(B) Claims 9-18, which depend from independent claim 1, stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Tong in view of teachings from U.S. Patent 6,650,019 to Glenn et al. (hereinafter "Glenn").

The claims of the above-referenced application are drawn to methods for forming protective layers on semiconductor device components. The method of independent claim 1 includes, among other things, subjecting at least the protective material to conditions that will heal cracks and delaminated areas that were formed as the components were severed. After the protective material is subjected to such conditions, the protective material is fully cured, *before* the resulting semiconductor device is assembled with another component of an electronic device.

It is respectfully submitted that, in the final rejections of the claims of the above-referenced application, the Examiner has erred in at least one respect: a *prima facie* case of obviousness has not been established because Tong and Glenn do not teach or suggest each and every element of independent claim 1. Specifically, neither Tong nor Glenn teaches or suggests a method in which a protective material is subjected to conditions that will heal cracks and delaminated areas of the protective material. Moreover, neither Tong nor Glenn teaches or suggests that protective material may be subjected to such conditions before the semiconductor device to which the protective material has been applied is assembled with another component of an electronic device.

Tong teaches that the B-stageable material is formulated so as to have a glass transition temperature that allows it to be "cleanly diced" once the material has been B-staged; *i.e.*, that the

material will not stick to the dicing saw or crack or break when sawed. Paragraph [0033].

Based on this teaching by Tong, there would be no reason for one of ordinary skill in the art to believe that there is any reason to heal cracks or delaminations of the "cleanly diced" B-staged material of Tong. Nor does Tong provide any teaching or suggestion in this regard.

In the process of Tong, a B-stageable material is applied to a semiconductor wafer (*see, e.g.,* paragraph [0013]), the B-stageable material is partially cured by removing solvent therefrom (*see, e.g.,* paragraph [0013]), the partially cured material and the wafer are diced (*see, e.g.,* paragraph [0013]), and a semiconductor device that has been coated with the partially cured B-stageable material is assembled face-down over a substrate before the B-stageable material is fully cured (paragraphs [0025] and [0026]). Tong does not teach or suggest that the B-stageable material may be fully cured *before* the semiconductor device is assembled with another component of an electronic device.

Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 1 is allowable over the teachings and suggestions of Tong.

Each of claims 2-23, and 25-29 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 8, which also depends from claim 5, is further allowable since Tong lacks any teaching or suggestion of applying the protective material such that the protective material is spaced apart from a base portion of at least one conductive structure.

Claim 25 is additionally allowable because Tong neither teaches nor suggests singulating semiconductor devices from a fabrication substrate once the material of a protective layer on the semiconductor devices has been singulated, then fully cured.

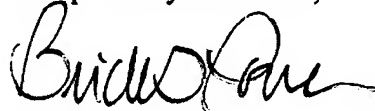
Claim 28 is further allowable because Tong includes no teaching or suggestion of healing the protective material by heating at least portions of a *thermoplastic material* located over peripheral regions of the adjacent semiconductor device components following severing and at least partially severing.

Withdrawal of the 35 U.S.C. § 103(a) rejections of each of claims 9-18 is respectfully solicited, as is the allowance of these claims.

CONCLUSION

It is respectfully submitted that the rejections of claims 1-23 and 25-29 are clearly erroneous and, as such, the Examiner has not met his burden in setting forth *prima facie* rejections against any of these claims. Accordingly, it is respectfully requested that the final rejections of claims 1-23 and 25-29 be reversed and that each of these claims be allowed.

Respectfully submitted,



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